An RFID-Based Guided Control Node for Batteryless Reconfigurable RF Architectures

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***Abstract*—This article introduces a passive reconfiguration strategy for RF networks based on radio frequency identification (RFID) integrated circuits (ICs) embedded within guided-wave structures. Each RFID IC is repurposed as a batteryless, addressable dc voltage source capable of biasing RF components, such as varactors and GaAs switches. Unlike conventional over-the-air (OTA) architectures, the proposed approach eliminates tag antennas by integrating the ICs directly into microwave transmission lines, where power, control, and signal share the same RF path. A dedicated multichip test platform is developed to experimentally characterize the IC behavior in this novel configuration, evaluating impedance variation, activation thresholds, and output stability. Measurements on a commercial RFID chip demonstrate reliable operation with only −15 dBm of incident RF power, and sufficient dc output to drive over 1000 GaAs SPST switches or 10 000 varactors. To validate the concept, a fully passive, four-element monopole array operating at 900 MHz is demonstrated, where each element is gated by an RFID-controlled SPST switch. The array performs beam steering through selective element activation, using a single RF feed to simultaneously energize the array, power the ICs, and transmit EPC Gen2 control commands.**

***Index Terms*—Batteryless voltage control, guided-wave radio frequency identification (RFID) architecture, reconfigurable networks.**

I. Introduction

THE growing demand for dynamic, adaptive, and energy-efficient control of electromagnetic radiation is driving research into novel paradigms of reconfigurable microwave networks. Applications ranging from 5G/6G communications to satellite payloads, radar sensing, wearables, and wireless power transfer (WPT) systems increasingly require beamforming and beam-switching capabilities that are not only programmable, but also compatible with constraints in power consumption, form factor, and scalability [1], [2], [3], [4].

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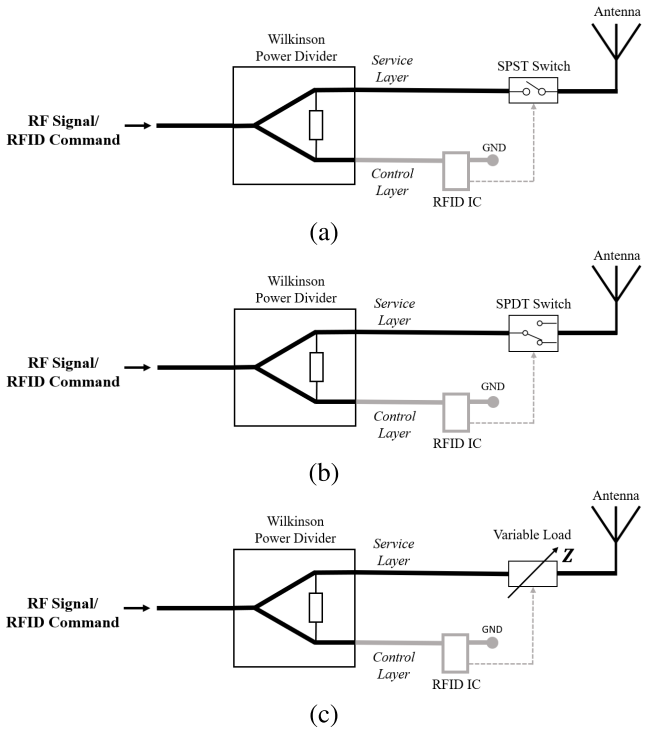


Fig. 1. Concept of guided RFID-based reconfiguration mechanisms, integrating the service and control layers in the same infrastructure. Depending on the programming state of the RFID IC, three scenarios are illustrated: (a) SPST switch for enabling or disabling specific RF paths, (b) SPDT switch for dynamic signal routing, and (c) variable load for introducing controlled phase shifts or delays along the line. Solid lines represent RF transmission lines, while dashed lines represent dc bias connections to the RFID IC.

Traditional architectures rely on electronically tunable components—such as PIN diodes, varactors, or GaAs switches—controlled by active platforms based on microcontrollers, field-programmable gate arrays (FPGAs), or dedicated beamforming ICs (BFICs) [5]. Although these systems enable fast and precise control of phase and amplitude, they require continuous power supplies, synchronized clocks, and digital control buses (e.g., SPI, I^2C). For instance, BFICs typically demand ~150 mW per channel, dual supply voltages, and careful routing and shielding to mitigate noise and crosstalk in dense arrays [6]. Their high cost—often hundreds of USD per chip—further limits deployment at scale [7]. As a result, active architectures are poorly suited for energy-autonomous,

low-cost, and massively distributed systems such as passive metasurfaces or long-lifetime sensor nodes [8], [9].

To overcome these limitations, recent studies have explored the use of radio frequency identification (RFID) integrated circuits (ICs) as ultralow-power actuators in reconfigurable electromagnetic devices [10]. Early implementations include programmable devices such as frequency selective surface (FSS) [11], reconfigurable intelligent surfaces [12], [13], reconfigurable antennas, and primary/secondary RFID tags [14]. In such systems, commercial RFID ICs are repurposed as passive, uniquely addressable controllers that harvest RF energy and generate local dc voltages to drive single-pole single-throw (SPST) and single-pole double-throw (SPDT) switches, or analog tunable elements such as varactors [15], [16]. Thanks to their electronic product code (EPC)-based addressing, these chips support asynchronous reconfiguration without centralized logic or wired interfaces.

Prior work has largely focused on over-the-air (OTA) RFID-controlled devices, where chips are coupled via external antennas. In contrast, the present work introduces a novel *guided-mode architecture*, in which RFID ICs are directly embedded into microwave transmission lines (such as microstrip networks or beamforming matrices) and operate as fully passive, addressable control nodes (Fig. 1). Each IC is integrated in parallel with the RF transmission path and harvests energy from the same guided wave that carries the service signal. This results in a dual-layer infrastructure: the *service layer*, delivering the functional RF signal, and the *control layer*, formed by the RFID nodes, are physically and functionally superimposed. This guided integration paradigm consolidates control, power delivery, and signal transmission into a single physical path, offering several advantages over conventional OTA RFID schemes.

1) Higher energy efficiency, as guided-wave propagation entails lower attenuation than free-space links, enabling the activation of multiple chips and reliable control overextended structures.
2) Minimal electromagnetic footprint, since inactive chips introduce negligible loading and do not distort the RF service signal.
3) Elimination of the OTA interface, which removes the need for tag antennas, reducing footprint, mechanical complexity, and detuning sensitivity.
4) Improved scalability and compactness, due to the absence of discrete radiators and external wiring, allowing dense integration of control nodes along the transmission line.
5) Low-loss architecture, as a single RF waveform concurrently powers the ICs, transmits control data, and supports system operation without additional coupling elements.

However, since RFID ICs have never been used in such guided-wave configurations, their performance in this role is unknown. This work, therefore, also reports a systematic experimental characterization of their RF and dc behavior, moving beyond standard identification metrics toward parameters relevant to power delivery, stability, and actuation.

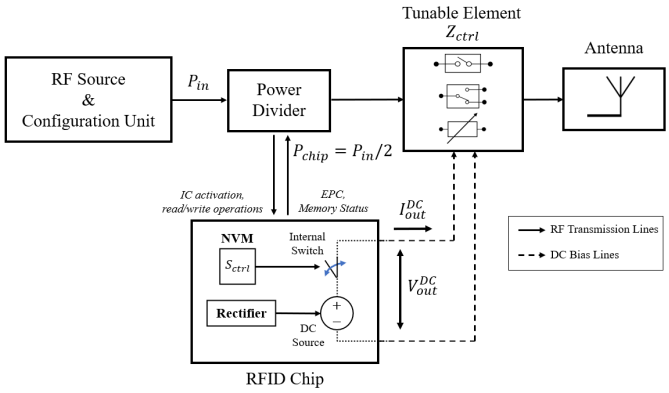


Fig. 2. Schematic representation of the network topology in the proposed RFID-based architecture. The RF source and configuration unit deliver both the service signal (modulated or unmodulated) and the EPC Gen2 programming commands through a shared RF path. A power divider routes part of the input signal ($P_{\text{chip}} = P_{\text{in}}/2$) to the RFID chip, which rectifies the carrier, retrieves the control bit S_{ctrl} from its NVM, and conditionally activates the internal dc source to bias the connected tunable element Z_{ctrl} (e.g., SPST/SPDT switch, variable load).

The remainder of this article is organized as follows. Section II introduces the notation and defines the main electrical quantities relevant to the RFID-based switching mechanism. Section III formalizes the conceptual framework of the guided-mode architecture and its operational regimes, highlighting the dual-layer infrastructure and the role of programmable RFID nodes in reconfiguring microwave networks. Section IV presents a detailed experimental method for characterization of the RFID chips, including their activation thresholds, output stability, impedance behavior, and current–voltage performance under various loading conditions. An example of the proposed architecture is given in Section V concerning a reconfigurable monopole antenna array operating at 900 MHz, capable of beam steering with a single RF feed.

II. Conceptual Architecture and Operating Principle

This section formalizes the proposed RFID-based reconfiguration mechanism, progressing from the single-node level to the full network architecture.

A. Programmable Node and Network Topology

The elementary building block is the *programmable node*, consisting of an RFID IC connected to one or more RF elements via its dc output. The chip acts as a batteryless, addressable voltage source: it harvests RF energy from an incident carrier and conditionally enables the output based on its internal memory state S_{ctrl}. The connected RF components (e.g., p-i-n diodes, SPST switches, varactors) are biased via $V_{\text{out}}^{\text{dc}}$, thereby altering their impedance Z_{ctrl} and locally reconfiguring the host RF system.

Fig. 2 illustrates a representative implementation. The RFID IC is embedded in a guided-wave structure and intercepts the same transmission line that conveys the operational signal, referred to as the *service layer*. From this line, the IC harvests energy and decodes EPC Gen2 programming commands, subsequently applying the appropriate dc bias to the connected RF

components, thus forming the *control layer*. Upon reception of a valid command, the chip stores S_{ctrl} in nonvolatile memory (NVM) and, when powered, supplies the corresponding dc output without the need for local supplies or digital controllers.

At the system level, the reconfigurable network is driven by two core modules.

1) *RF Source:* Generates the service signal with input power P_{in}. It acts as both a functional stimulus and an energy source for all ICs.
2) *Configuration Unit:* Implements EPC Gen2 via amplitude shift keying (ASK) modulation. It may be integrated in the RF source or realized via a dedicated RAIN RFID reader.

The full system comprises N programmable nodes distributed along the RF infrastructure. Each node, indexed as $\text{IC}_1, \text{IC}_2, \ldots, \text{IC}_N$, controls a group of K elements sharing the same bias state. As each IC stores one bit S_{ctrl}, the system can realize 2^N reconfiguration states with local 1-bit granularity.

B. Operational Principle and Frequency Regimes

Each programmable node operates through three sequential tasks.

1) *Programming:* The RFID chip is addressed via an RF carrier modulated with EPC Gen2 commands at frequency f_p. Upon successful decoding, the chip stores a control bit S_{ctrl} in its NVM. This phase requires the received power to exceed the write threshold, i.e., $P_{\text{chip}} \geq P^{w}_{\text{chip}}$.
2) *Activation:* When powered by any RF signal (modulated or not modulated) at frequency f_s with $P_{\text{chip}} \geq P^{\text{op}}_{\text{chip}}$, the chip rectifies the input, accesses the stored value S_{ctrl}, and enables the dc output accordingly. If $S_{\text{ctrl}} = 1$, a voltage $V^{\text{dc}}_{\text{out}} = V^{\text{ON}}$ is supplied; otherwise, the output remains in a high-impedance state, V^{OFF}.
3) *Actuation:* The dc output biases an RF component, switching its impedance between $Z^{\text{ON}}_{\text{ctrl}}$ and $Z^{\text{OFF}}_{\text{ctrl}}$, thereby reconfiguring the electromagnetic behavior of the host system.

The programming phase is asynchronous and infrequent, as the stored control bit persists across multiple activation cycles. In contrast, activation and actuation are continuous during normal operation, requiring uninterrupted RF powering to maintain the desired impedance state.

Three distinct frequencies define the system's operation.

1) *Programming Frequency* f_p: carries the modulated EPC Gen2 command.
2) *Power-Up Frequency* f_s: supplies RF energy for chip activation.
3) *Operating Frequency* f_0: corresponds to the functional RF task (e.g., beamforming).

Based on their relationship, the system can operate in three regimes.

1) *Fully Decoupled Regime* ($f_p \neq f_s \neq f_0$): Enables high flexibility, e.g., RFID-based reconfiguration in mmWave systems, but requires more complex synchronization and filtering.
2) *Hybrid Regime* ($f_p \neq f_s = f_0$ or $f_p = f_s \neq f_0$): The service signal acts as both a functional waveform and a power source; programming remains spectrally separated and may be performed offline.
3) *Fully Integrated Regime* ($f_p = f_s = f_0$): A single UHF carrier simultaneously supports powering, programming, and RF operation. This simplifies the architecture and supports in-line reconfiguration via standard Gen2 readers, provided that f_0 lies within the RFID band. However, recent studies have shown feasibility beyond UHF through Gen2-compliant SDR platforms [17], [18], [19].

The selection of the regime should be driven by application-specific constraints, including frequency band, power budget, and integration level.

III. Characterization of Passive RFID ICs for Guided-Mode Control

In guided-mode RF networks, passive RFID chips are repurposed beyond their standard identification role, functioning as embedded dc voltage sources directly integrated within transmission lines. This dual functionality, particularly the actuation task, forces the chips to operate outside typical manufacturer-specified conditions. As a result, conventional datasheet parameters such as read sensitivity and nominal input impedance are inadequate to predict system behavior or ensure reliable performance in guided-mode configurations.

A dedicated experimental characterization is therefore required to extract the following critical performance metrics.

1) *Power-dependent input impedance*, to quantify how Z_{chip} varies with incident RF power and to assess its implications for impedance matching and power transfer;
2) *Operation sensitivity* $P^{\text{op}}_{\text{chip}}$, defined as the minimum RF power required to generate a usable dc output across representative electrical loads;
3) *dc output characteristics*, including the current–voltage (I–V) response, the maximum deliverable power, and the trade off between actuation performance and EPC Gen2 protocol functionality.

Sections III-A–III-D detail the measurement setup and protocol developed to extract these parameters. After presenting the general methodology applicable to any passive RFID IC, the approach is applied to a specific case study.

A. Test Board Design

The experimental setup relies on a custom multichip evaluation board, conceptually illustrated in Fig. 3. The board implements a parallel configuration of N RFID ICs, each functioning as an independently addressable control node embedded in a shared RF transmission line. This architecture emulates the physical conditions of guided-mode networks and allows simultaneous characterization of multiple chips under identical excitation. Each IC is connected to a dedicated impedance matching network designed to transform its nominal impedance Z_{chip} to an intermediate value $Z_{\text{match}} = N \cdot Z_0$, where Z_0 is the system reference impedance (typically $50\,\Omega$).

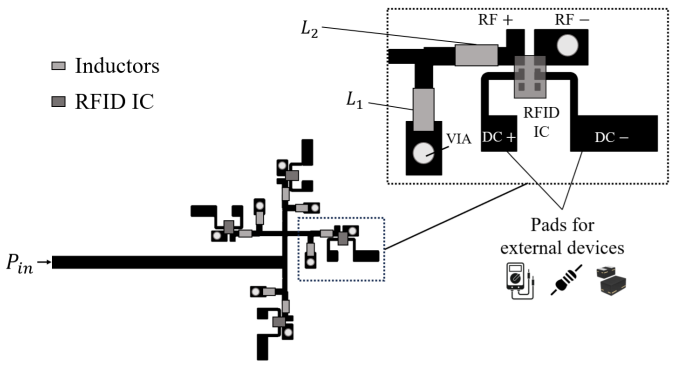


Fig. 3. Scheme of the proposed layout for IC testing and characterization. In this conceptual illustration, $N = 4$ ICs are considered.

Compact lumped-element L-networks, comprising two inductors L_1 and L_2, are used to minimize footprint and support post-fabrication tuning.

The board offers RF and dc access points to support a broad range of instrumentation.

1) A vector network analyzer (VNA) for S_{11} and impedance measurements.
2) A UHF RFID reader for EPC Gen2 programming and control.
3) A software-defined radio (SDR) for custom waveform testing and advanced modulation.

Moreover, each IC features dedicated dc output pads for connection to.

1) Oscilloscopes or source-meter units (SMUs) for voltage and I–V characterization.
2) Programmable electrical loads (resistive or reactive) to emulate actuation scenarios.

The effective power received by each chip is estimated from the input power P_{in} and the measured reflection coefficient S_{11} as:

$$P_{\text{chip}} = P_{\text{in}} - M - P_{\text{split}} \tag{1}$$

where $M = -10\log_{10}(1-|S_{11}|^2)$ accounts for mismatch losses, and $P_{\text{split}} = 10\log_{10}(N)$ accounts for ideal power division among N branches.

B. Power-Dependent Input Impedance

The input impedance of passive RFID ICs varies nonlinearly with incident RF power due to internal transitions in rectification and logic circuits [20]. This dependence can significantly affect matching performance, especially in guided configurations with low propagation losses, high signal levels, and strong fields.

To investigate this behavior, S_{11} must be measured across a sweep of input power levels P_{in} from P_{min} to P_{max}, at fixed frequency f_0 and representative of the system carried signals. For each step, the power received by each IC, P_{chip}, is estimated using (1). The evolution of S_{11} as a function of P_{chip} reveals the transition from the chip's inactive (high-Z) state to the active regime, where power is absorbed by the rectifier and digital blocks. This analysis informs the optimal operating range and matching design under varying signal strengths.

C. Operation Sensitivity

The operation sensitivity $P_{\text{chip}}^{\text{op}}$ is defined as the minimum incident RF power at which the chip generates a stable and usable dc voltage across an attached load. Unlike conventional read/write thresholds, this metric is strongly load-dependent and must be measured for each application scenario.

The procedure consists of sweeping P_{in} while monitoring the corresponding dc output voltage $V_{\text{out}}^{\text{dc}}$ using an oscilloscope or SMU instrumentation. The power delivered to the chip, P_{chip}, is again computed from (1). For each load condition, the minimum P_{chip} yielding full activation defines the operation sensitivity. This measurement allows the designer to select suitable actuation components and to determine the field strength requirements for robust passive operation.

D. DC Output Characterization

To fully assess the RFID chip's capability as a dc voltage generator, its I–V behavior is characterized under load. In addition to identifying the maximum deliverable power, this test determines whether EPC Gen2 communication and actuation can coexist under given load conditions.

The measurement consists of applying a fixed-power CW excitation, alternated with EPC commands, while varying the external load resistance. For each load, the steady-state voltage and current at the dc output terminals are recorded. The chip's responsiveness to EPC memory access is verified in parallel to identify the boundary between actuation-only and dual-function operation. The resulting I–V curve reveals.

1) The maximum usable output power $P_{\text{out}}^{\text{dc}}$.
2) The voltage regulation profile under increasing load current.
3) The operational limit where power delivery inhibits digital communication.

These insights are crucial for balancing power distribution between logic and actuation subsystems in guided RFID architectures.

E. Application Example

The previous methodology is here applied to the characterization of the EM4152 chip [15], which is the only commercially available UHF RFID IC known to autonomously provide a dc bias voltage without internal energy storage or external regulation. This makes it a representative benchmark for evaluating the feasibility of batteryless guided-mode control architectures. From a circuit-level perspective, the EM4152 follows the canonical structure of a passive UHF RFID IC [21], [22]. Its analog front-end comprises a rectifier and power management unit for RF-to-dc conversion, a demodulator for downlink data detection, and a modulator that varies the chip input impedance to enable backscatter communication. Unlike standard ICs, a fraction of the rectified dc power can be routed to the external pads. The RF input can be modeled as a parallel RC network, whose impedance at 900 MHz under minimum-power excitation is $Z_{\text{chip}} = 17.6 - j271.9\,\Omega$. Moreover, the chip exhibits a read sensitivity of $P_{\text{chip}}^{r} = -18\,\text{dBm}$ and a write sensitivity of $P_{\text{chip}}^{w} = -13\,\text{dBm}$ [15].

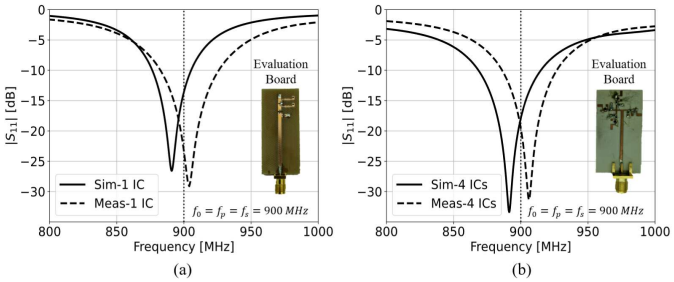


Fig. 4. Measured S_{11} of the evaluation boards with $P_{\text{in}} = -20\,\text{dBm}$. (a) Single-chip board. (b) Multichip ($N = 4$) board.

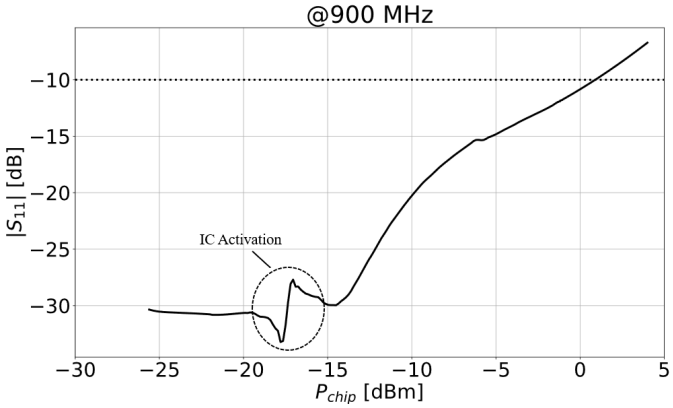


Fig. 5. Measured S_{11} of the evaluation board as a function of the RF power reaching the IC at $f = 900\,\text{MHz}$. The abrupt transition indicates the activation of the RFID ICs.

The custom evaluation board was designed in AWR Microwave Office and fabricated on a Rogers RO4003C substrate ($\varepsilon_r = 3.55$, $\tan\delta = 2.1 \cdot 10^{-3}$, 1.6 mm thick [23]). Two configurations were realized and characterized: the first embedding $N = 1$ EM4152 IC matched to 50 Ω through a lumped-element L-network composed of two series inductors ($L_1 = 1.5\,\text{nH}$, $L_2 = 23\,\text{nH}$), and the second integrating $N = 4$ parallel-connected EM4152 ICs, each individually matched to 200 Ω under the same conditions but with different tuning inductors ($L_1 = 19\,\text{nH}$, $L_2 = 15\,\text{nH}$) to ensure equal power distribution among them.

Fig. 4 shows the fabricated prototypes and the comparison between simulated and measured reflection coefficient S_{11} of both the single- and multichip boards, evaluated through the Pico108 VNA [24] with $P_{\text{in}} = -20\,\text{dBm}$. Although a slight detuning is visible, the matching at 900 MHz is pretty in line with the expectation in both cases.

Fig. 5 shows the measured reflection coefficient S_{11} of the test board as a function of the estimated chip power P_{chip} at 900 MHz. In the low-power regime ($P_{\text{chip}} < -20$ dBm), S_{11} remains consistently below $-30\,\text{dB}$, indicating stable chip impedance and effective matching. A marked variation in the S_{11} is observed near the read sensitivity threshold ($P^r_{\text{chip}} = -18$ dBm), corresponding to the onset of rectifier activation. Beyond this point, the chip begins to draw current from the RF input, resulting in a shift of its input impedance [25]. As P_{chip} increases, this behavior leads to progressive mismatch, with S_{11} rising but remaining below $-10\,\text{dB}$ up to approximately 0 dBm. The transition confirms the nonlinear impedance response of the EM4152 chip in its active state. Despite this, the board maintains acceptable matching across a broad dynamic range. However, in large-scale guided-mode networks, the observed sensitivity to power levels suggests that layout asymmetries and power routing strategies must be carefully considered to avoid nonuniform node activation.

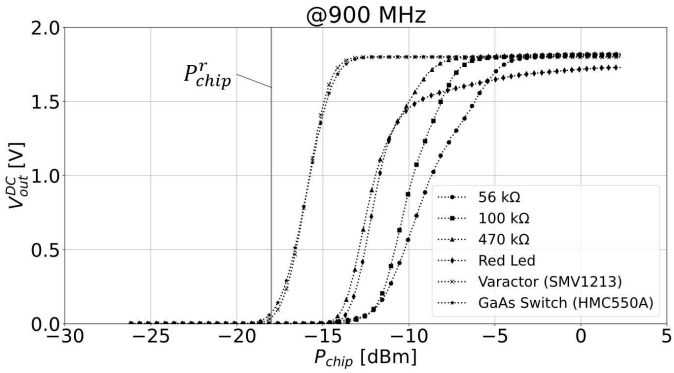


Fig. 6. Measured dc output voltage as a function of the RF power reaching the IC at $f = 900\,\text{MHz}$ for various loads.

Fig. 6 reports the measured dc output voltage $V^{\text{dc}}_{\text{out}}$ of one of the EM4152 ICs as a function of the estimated received RF power P_{chip}, under a representative set of electrical loads and for a CW input. The results indicate that tunable components such as varactors and GaAs SPST switches achieve stable dc activation at $P_{\text{chip}} \approx -15\,\text{dBm}$, slightly higher than the chip's nominal read sensitivity. These components draw limited current and are therefore compatible with the low power budget of passive RFID ICs. In contrast, resistive loads with lower resistance values require significantly higher P_{chip} to sustain a comparable voltage. For instance, a $56\,\text{k}\Omega$ load only reaches activation for $P_{\text{chip}} > -8\,\text{dBm}$. This highlights the dependence of operation sensitivity on the load's current demand. Moreover, in all tested configurations, the output voltage exhibits a plateau behavior: once activated, the voltage remains approximately constant at $V^{\text{ON}}_{\text{out}} \approx 1.8$ V despite further increases in P_{chip}. This ensures stable actuation and predictable response over a wide dynamic range, provided the load remains within the chip's power budget.

Finally, the measured I–V response of the EM4152 RFID chip under continuous-wave excitation at $P_{\text{in}} = 0\,\text{dBm}$ reveals a nonlinear behavior. The output voltage varies from below 1 V to a maximum value of approximately 1.85 V, depending on the connected electrical load. The corresponding maximum output power reaches $P^{\text{dc,max}}_{\text{out}} \approx 550\,\mu\text{W}$, confirming the chip's ability to deliver useful power to external components without any auxiliary energy source. A key outcome of this analysis is the identification of a specific *operative region*, highlighted in Fig. 7, in which both dc generation and EPC Gen2 communication are simultaneously supported. Within this region, the harvested RF energy is sufficient to power the digital control logic and generate a stable dc output. Outside this window, although the chip continues to supply voltage to the load, its communication capability degrades due to insufficient residual power for digital operations and backscatter response.

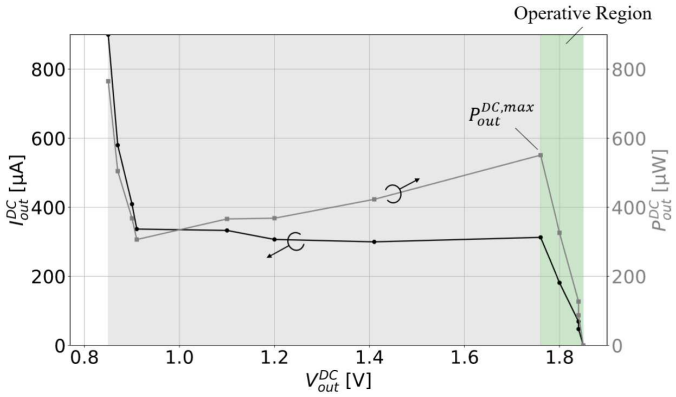


Fig. 7. Measured *I–V* characteristic of the RFID chip's dc output under 0 dBm CW excitation. The shaded green area indicates the operative region where both dc generation and EPC memory access are supported.

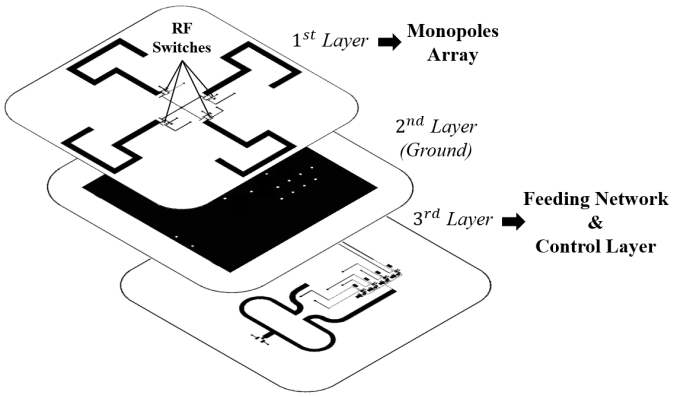


Fig. 8. Multilayer architecture of the RFID reconfigurable monopole array. Physical connections are schematized in Figs. 9(b) and 10(b).

TABLE I

TYPICAL DC BIASING REQUIREMENTS FOR REPRESENTATIVE TUNABLE COMPONENTS AND ESTIMATED MAXIMUM NUMBER OF ELEMENTS *N* THAT CAN BE SIMULTANEOUSLY DRIVEN BY A SINGLE RFID IC

	Varactor	**GaAs Switch**	**PIN Diode**
V_{th} $[V]$	/	1.6	0.7
I_{DC} $[nA]$	20	200	1000 - 10000
P_{DC} $[\mu W]$	0.037	0.37	700 - 7000
K	**12000**	**1200**	**0**

TABLE II

GEOMETRICAL DIMENSIONS OF THE RADIATING ELEMENTS

Physical Dimensions [mm]								
l_1	l_2	l_3	l_4	l_5	l_6	l_{GND}	w_1	w_2
12	30	12	16	30	16	79	3	0.5

TABLE III

GEOMETRICAL DIMENSIONS AND LUMPED COMPONENTS OF THE RF NETWORK

Physical Dimensions [mm]							**Lumped Components [nH]**	
l_1	w_1	l_2	w_2	l_3	l_4	R	L_1	L_2
8.0	2.5	14.0	2.0	8.0	18.0	7.0	5.0	24.0

To assess component compatibility, Table I compares the chip's output capability with the typical dc requirements of various tunable elements. Varactors, which typically demand less than 50 nW, can be driven in large arrays (up to $K = 12000$ elements per chip) without exceeding the power budget. GaAs switches, requiring approximately $0.37\,\mu W$ each, are also well supported, with an estimated $K \approx 1200$ devices controllable in parallel. In contrast, PIN diodes require significantly higher current (1–10 μA), making them incompatible with fully passive RFID control under the tested conditions. Moreover, it should be highlighted that the parameter K in Table I expresses the *theoretical* scalability limit of the proposed architecture, derived from the balance between the maximum dc power deliverable by the RFID chip and the power consumption of the external loads.

IV. APPLICATION EXAMPLE: RECONFIGURABLE MONOPOLE ARRAY

To demonstrate the feasibility and performance of the proposed guided RFID architecture in a practical RF scenario, a fully passive reconfigurable antenna array was designed, fabricated, and experimentally validated. The implemented prototype, borrowed from [26], consists of a four-element monopole array operating at 900 MHz where the beam steering capability is achieved via selective activation of the radiating elements through RFID-controlled switches. All system functions, including powering, programming, and RF operation, occur at the same frequency ($f_p = f_s = f_0 = 900$ MHz).

The antenna system is implemented on a multilayer printed circuit board (PCB) using standard FR-4 laminates ($\varepsilon_r = 4.3$, $\tan\delta = 0.025$, thickness 1.6 mm). The structure consists of three functional layers (Fig. 8): 1) the top layer hosts the four quarter-wave monopole antennas; 2) the intermediate layer serves as a common ground plane; and 3) the bottom layer integrates the RF power divider and the control circuitry, including the embedded RFID chips.

A. Radiating Elements

The top layer of the array hosts four identical quarter-wavelength monopoles, each designed for resonance at 900 MHz and implemented as copper strips printed above a shared ground plane, as shown in Fig. 9(a). The monopoles are arranged in a cross-like configuration, physically rotated by 90° with respect to one another to enable directional beam steering along the principal axes. It is worth noting that, even though the considered reconfigurable array requires just a single monopole activated at a time, the proposed RFID network would be capable of simultaneously handling multiple active elements without any significant performance degradation.

Each monopole is connected to a central microstrip feed line through a GaAs SPST switch (HMC550A [27]) and a dc blocking capacitor ($C = 500$ pF) to preserve the dc bias while maintaining RF continuity [Fig. 9(b)]. The switches serve as controllable RF gates and are individually biased by the local

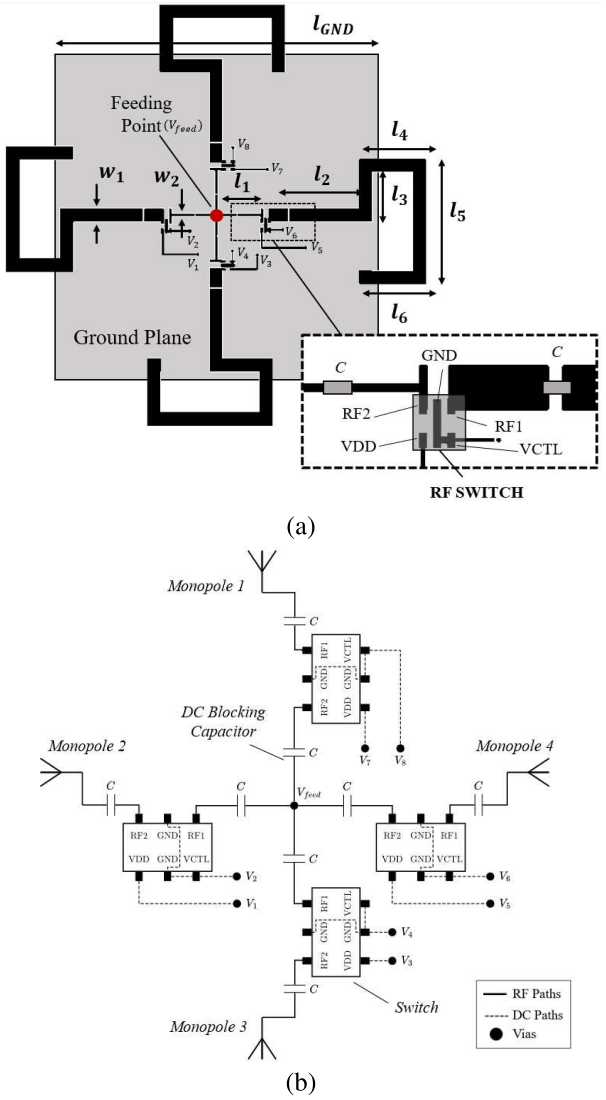


Fig. 9. (a) Layout of the reconfigurable monopole array, featuring four quarter-wavelength monopoles arranged in a cross configuration above a common ground plane. Each monopole is connected to the central feed line via a GaAs RF switch, enabling individual excitation under RFID-based control. Dimensions are listed in Table II. (b) Corresponding schematic representation where solid lines represent RF paths, dashed lines represent dc paths, and black dots are for vias. Connections between layers are indicated with $V_{\text{feed}}, V_1, \ldots, V_8$.

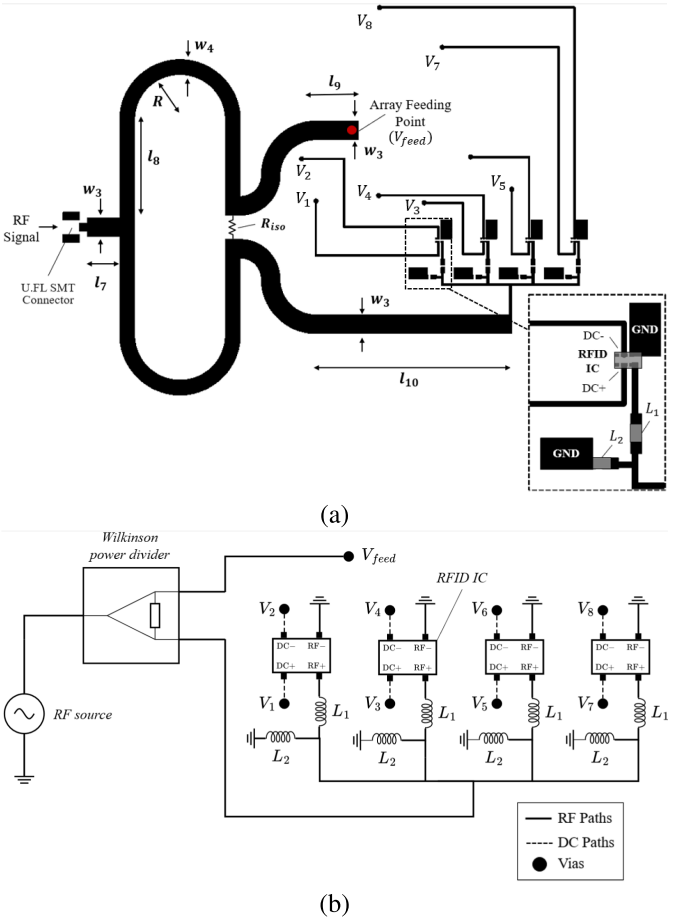


Fig. 10. (a) Layout of the RF feeding network, featuring a Wilkinson power divider. The control branch includes four parallel RFID ICs, each matched to 200 Ω via L-networks. Details in Table III. (b) Corresponding schematic where solid lines represent RF paths, dashed lines represent dc paths, and black dots are for vias. Connections between layers are indicated with $V_{\text{feed}}, V_1, \ldots, V_8$.

dc voltage generated by a dedicated EM4152 RFID chip. When $V_{\text{out}}^{\text{dc}} = 0\,\text{V}$ (i.e., $S_{\text{ctrl}} = 0$), the corresponding switch is closed, and the associated monopole is directly excited by the feed line. Conversely, when $V_{\text{out}}^{\text{dc}} = 1.8\,\text{V}$ ($S_{\text{ctrl}} = 1$), the switch remains open, isolating the monopole from the excitation. Thus, by closing only one switch at a time, a single monopole becomes the active radiating element, while the remaining elements behave as parasitic scatterers. The resulting electromagnetic interactions enable four-state beam switching toward the cardinal directions.

B. RF Network Topology

The embedded RF network [Fig. 10(a)] is designed to simultaneously deliver the service signal to the antenna and the power/programming signals to the RFID-based control system. A two-way Wilkinson power divider, operating at 900 MHz, splits the input RF signal into two equal-power branches. One output feeds the service layer and provides the excitation for the active radiating element. The second branch, the control layer, powers and programs the RFID ICs that are responsible for enabling or disabling the switches associated with each antenna element. To minimize signal leakage and mutual interference between branches, an isolation resistor $R_{\text{iso}} = 100\,\Omega$ is placed at the junction [28].

In the control branch [Fig. 10(b)], $N = 4$ EM4152 RFID ICs are connected in parallel to the transmission line. Each chip is individually matched to 200 Ω via compact L-network matching circuits, resulting in an effective input impedance of approximately 50 Ω. This arrangement guarantees impedance continuity along the control path and equal power distribution among the ICs. The dc outputs of the chips are routed to the corresponding SPST GaAs switches placed in the radiating layer. This strategy allows each switch, and thus each antenna element, to be independently activated by means of the RFID protocol. Due to the half-power division and the parallel configuration of four ICs, each chip receives approximately 1/8 of the total input power. Hence, assuming ideal matching

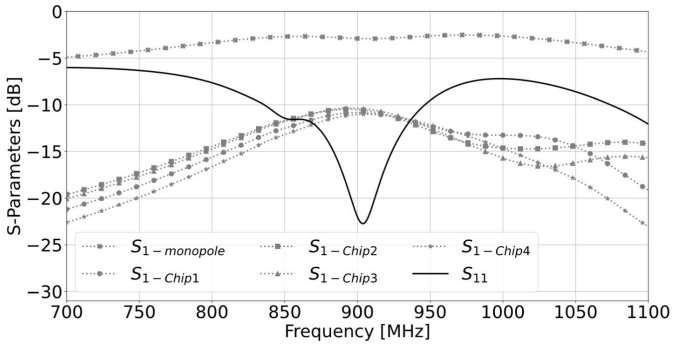


Fig. 11. Simulated S-parameters of the reconfigurable array. The plot shows the input matching (S_{11}) and the power coupling toward the monopole array and each RFID-controlled branch.

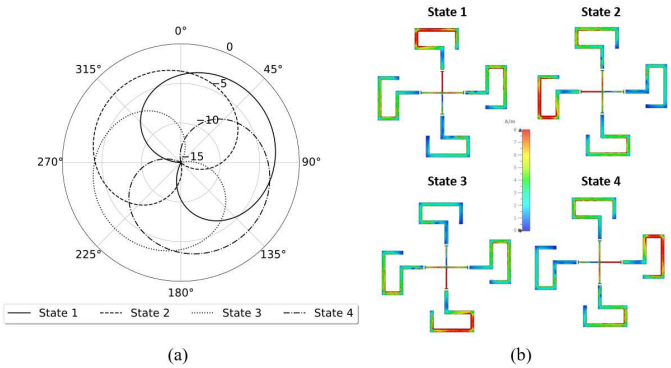


Fig. 12. Simulated beam-switching behavior of the RFID-controlled monopole array. (a) Far-field patterns in the azimuthal plane for each switching state. (b) Surface current distributions corresponding to the active element in each state.

and equal division, the minimum input power required to ensure full activation of the control circuitry and proper dc power delivery is estimated as $P_{\text{in}}^{\text{min}} = -6\,\text{dBm}$.

C. Numerical Analysis

All geometrical and matching parameters of the RFID-reconfigurable monopole array and of the network were numerically optimized in CST Microwave Studio 2025.

The simulated S-parameters in Fig. 11 confirm excellent impedance matching at the input port, with the return loss S_{11} remaining below $-20\,\text{dB}$ at the operating frequency $f = 900\,\text{MHz}$. As expected, approximately half of the input power is routed to the monopole array feed line ($S_{1\rightarrow\text{Monopole}} \approx -3\,\text{dB}$), consistent with the design of the Wilkinson power divider. The scattering parameters $S_{1\rightarrow\text{Chip1}}$ through $S_{1\rightarrow\text{Chip4}}$ indicate that each RFID chip receives close to $-10\,\text{dB}$ of the total input power, as predicted by the theoretical division ($-3\,\text{dB}$ at the Wilkinson output and $-6\,\text{dB}$ due to four parallel branches). Small variations among the chips, visible outside the operational band, are attributed to differences in transmission line lengths and parasitic effects introduced by layout asymmetries. Nevertheless, these variations do not significantly impact performance within the operating frequency range, where power distribution and matching remain well balanced.

To assess the beam-switching functionality, the array was simulated under the four distinct switching states, each corresponding to the activation of a single monopole while the others remain disconnected. Fig. 12(a) shows the resulting far-field radiation patterns in the *xy*-plane, demonstrating clearly separated main lobes pointing in the cardinal directions. Complementary surface current distributions are shown in Fig. 12(b). Each configuration highlights the dominance of the active monopole, with strong current localization on the excited element and weaker induced currents on the passive monopoles, which function as parasitic directors or reflectors depending on the spatial configuration.

D. Experimental Validation

The prototype of the RFID-reconfigurable monopole array (Fig. 13) was fabricated by etching 1.6 mm-thick FR-4 PCBs and assembling two stacked layers, with all passive components and SPST switches soldered in place. Copper vias ensured vertical interconnections between layers.

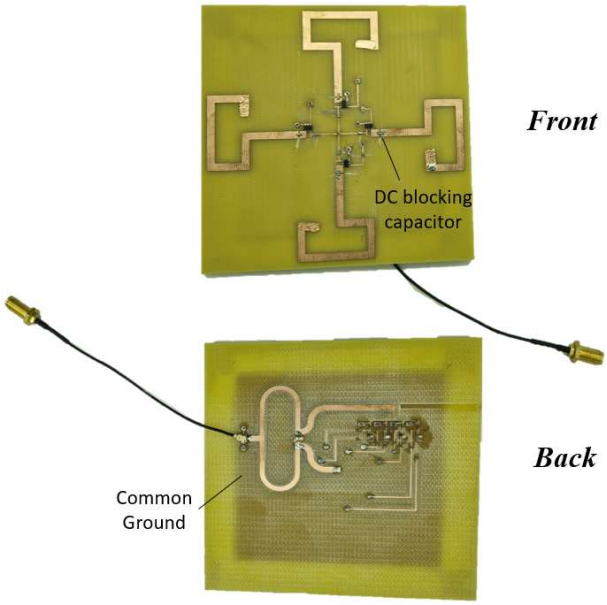
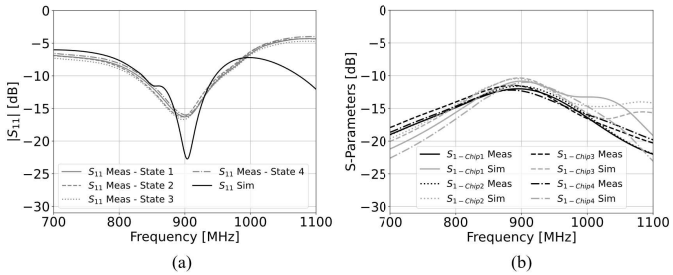


Fig. 13. Fabricated RFID-reconfigurable monopole array prototype. The front view shows the monopole layer with soldered SPST switches and dc-blocking capacitors. The back view highlights the Wilkinson power divider and common ground plane.

1) Reflection Coefficient Measurements: The input reflection coefficient S_{11} of the assembled prototype was measured through a VNA, with only one monopole activated at a time via RFID reprogramming. Fig. 14(a) compares the measured and simulated S_{11} traces, confirming proper impedance matching around 900 MHz in all operating states. To assess the actual RF power reaching each RFID IC, the Voyantic Tagformance UHF Pro system [29] was used to identify the activation threshold of each chip. By following the turn-on method, the system performs a frequency sweep while gradually increasing the input power P_{in} until the chip begins responding. Since chip activation occurs when $P_{\text{chip}} = P_{\text{chip}}^{r}$, the corresponding transmission coefficient from the input to each chip, S_{1j} (with



(a) (b)

Fig. 14. Measured and simulated S-parameters of the reconfigurable monopole array. (a) Reflection coefficient S_{11} for each activation state compared to simulation. (b) Measured and simulated transmission coefficients S_{ij} between the feed port and each RFID chip.

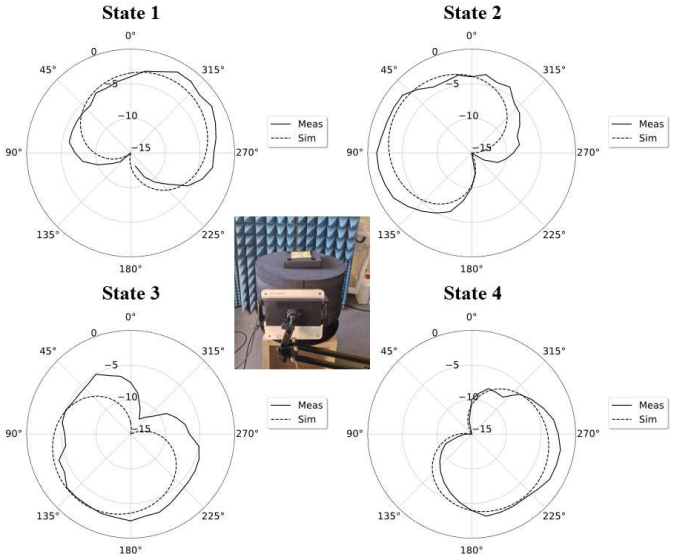


Fig. 15. Measured and simulated radiation patterns in the azimuthal plane at 900 MHz for each beam-steering state (States 1–4), with the prototype programmed to activate a single monopole per configuration. In the inset, the measurement setup with the reference antenna and rotating platform used for angular scanning.

$j = 1, \ldots, 4$), can be estimated as

$$S_{1j} = P^{r}_{\text{chip}} - P_{\text{in}} - L_{\text{cables}} \tag{2}$$

where $L_{\text{cables}} = 3$ dB accounts for the insertion loss of the coaxial cabling. The measured values, reported in Fig. 14(b), are in close agreement with the simulated transmission coefficients, validating the correct distribution of power among the RFID chips. Minor discrepancies are attributed to manufacturing tolerances, connector losses, and small asymmetries in the layout.

2) Reconfigurable Radiation Pattern Measurements: The far-field radiation characteristics were evaluated using a single-axis measurement setup (Fig. 15). The array was positioned horizontally on a rotating foam platform to enable discrete angular sampling of the azimuthal radiation pattern. A circularly polarized receiving antenna (Keonn CP patch) was placed at a fixed distance $d = 50$ cm, within the far-field region, and connected to the VNA to record the transmission coefficient S_{21}.

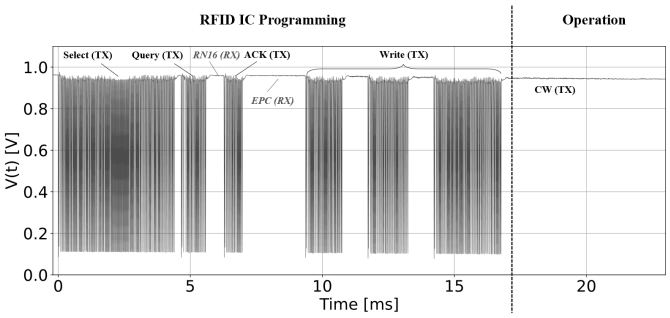


Fig. 16. Oscilloscope trace of the EPC Gen2 signal transmitted by the ThingMagic reader, showing the Select, Query, ACK, and Write commands sent during the programming phase [30] and the CW transmission during the operation phase. Unmodulated CW windows between commands are for powering the IC while it is responding.

Before each measurement, the RFID ICs were selectively reprogrammed using the ThingMagic M6E UHF RFID reader, sending EPC Gen2 commands (Fig. 16) to activate the desired SPST switch. Fig. 15 presents the measured radiation patterns at 900 MHz for all the beam states, overlaid with the simulated curves. Each configuration yields a directional beam steered toward a distinct quadrant, with an angular separation of approximately 90°, as expected. The measured patterns exhibit good agreement with simulations, with minor deviations ascribed to soldering asymmetries and perturbations introduced by the coaxial cable. However, it is important to note that the same RF port was used for both programming and measurement.

V. Conclusion

The presented study has demonstrated that commercial passive RFID ICs, when embedded into guided-wave structures, can serve as addressable, batteryless control units for RF reconfiguration. A key outcome of the work is the identification of the EM4152 chip as a viable enabler of this concept, provided that its electrical behavior—especially in terms of power sensitivity and dc output characteristics—is carefully modeled and matched to the target application.

The experimental characterization clarified the conditions under which the chip can simultaneously support memory access and actuation, revealing a well-defined operative region in the current–voltage domain. This dual-function behavior, communication and control, has not been systematically quantified in previous literature and constitutes a fundamental insight for future designs. The validation on a reconfigurable monopole array, operating in the fully integrated regime ($f_p = f_s = f_o$) and with a CW excitation as the service signal, confirmed the feasibility of beam switching using only passive elements and a unified RF path for power, control, and signal routing. It also demonstrated that stable RF operation can be preserved even when the programmable nodes are directly loaded onto the transmission line.

Despite these promising results, the study also clarifies two important design limitations. First, the output voltage is volatile and vanishes when RF power is removed, meaning that, although the control bit is nonvolatile, the chip must remain powered to sustain actuation. Second, the dc power budget is inherently modest, which restricts compatibility to

low-power components such as varactors and GaAs switches, while excluding higher current loads like PIN diodes. Another critical aspect requiring further investigation is the impact of signal modulation on chip behavior. Since the same RF signal may carry both user data and power, unintended interactions (such as backscatter), induced spectral contamination, or bias instability due to amplitude fluctuations, could arise in practical systems. Moreover, when the programming, power-up, and operating frequencies coincide ($f_p = f_s = f_o$), the temporal dynamics of Gen2 communication (e.g., carrier interruptions for command encoding) may interfere with service continuity.

Thus, future research will explore the operation of the proposed architecture under realistic modulated service signals (e.g., RFID, Wi-Fi, Bluetooth, and 5G). Further efforts will also explore fast wake-up strategies and multibit chip architectures to enhance control granularity. Moreover, while operation in the hybrid regime ($f_p = f_s \neq f_o$) has already been demonstrated by the authors in [31], a fully decoupled implementation ($f_p \neq f_s \neq f_o$) will be pursued in future studies. Finally, efforts will also focus on high-frequency embedding strategies to preserve sensitivity beyond the UHF band, enabling application to advanced platforms such as reconfigurable intelligent surfaces, spaceborne antennas, and next-generation wireless access points.

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